

LOW NOISE MONOLITHIC Ka-BAND P-HEMT AMPLIFIER FOR SPACE APPLICATIONS

B. Aja, M.L. de la Fuente, J.P. Pascual, A. Mediavilla, E. Artal

Dpto. Ing. de Comunicaciones. University of Cantabria
Avda. Los Castros s/n 39005 Santander. Spain

Phone: 34 – 942201391 ext.11 Fax: 34 – 942201488 e-mail: beatriz@dicom.unican.es

ABSTRACT

A monolithic P-HEMT Ka-band low noise amplifier is reported. This circuit was developed for being used in the Back End module of the differential radiometers in the European Scientific mission Planck. An average noise figure of 2.3 dB from 28 to 36 GHz with an associated gain greater than 20 dB was measured, and it achieved a minimum noise figure of 1.8 dB at 29.5 GHz. The amplifier provided 28 dB of gain from 29.5 GHz to 32 GHz.

INTRODUCTION

Monolithic millimeter-wave integrated circuits provide significant advantages of small size, and repeatability over the conventional hybrid integrated circuit components in millimeter-wave radar and radiometer system applications. The low noise amplifier (LNA) is a key component in these systems

This paper describes the design and assembly of a Ka-band low noise amplifier, which was developed as a part of the Back End Module for the Planck Low Frequency Instrument (LFI) receiver. The Planck LFI will have the sensitivity to measure cosmic microwave background anisotropies in the frequency range 30 – 100 GHz and it will be split into 4 channels centered at 30 GHz, 44 GHz, 70 GHz and 100 GHz. One of the main specifications for the amplifier design is the noise figure which must be low, since the instrument will be looking at background noise and its inherent noise must be as low as possible.

The amplifier is fully monolithic and the technology chosen has been OMMIC ED02AH process, which employs a 0.2 μm Pseudomorphic-High Electron Mobility Transistor (P-HEMT). Two transistor types are available, depletion mode and enhancement mode. In this design depletion mode transistors with a gate width of $6 \times 15 \mu\text{m}$ have been used in each stage of the amplifier.

CIRCUIT DESIGN

The design of the amplifier consists of four stages and there was some trade off between noise figure, input/output match and gain and the other important considerations were overall stability at all frequencies and flat gain over the operating bandwidth. The four-stage design is split into one low noise input stage and three gain flatness stages. A schematic of the Ka-band four-stage MMIC low noise amplifier is shown in Figure 1. The first stage uses inductive source feed back to achieve a low noise performance [1] with reasonable gain and return loss. Because of the natural roll-off in gain with frequency that occurs in the transistor, parallel feedback [2,3] has been used in the last three stages to give an upward slope to the gain. This feedback uses a resistor, an inductor and a blocking capacitor in series as a feedback path from the gate of the transistor to the drain and it has a minimal impact on noise figure. Parallel feedback has the advantage of increasing the stability factor, improving input and output return losses and flattening gains over widebands.

The amplifier was designed using MDS (Agilent) simulator and its electromagnetic quasi-3D tool was employed for the passive networks. Figure 2 shows a photograph of the four-stage MMIC low noise amplifier. The chip size is $3 \times 1 \text{ mm}^2$.

ASSEMBLY

The circuit has been measured in a homemade test fixture. Ridged waveguide (WR-28) [4] own designed transitions have been used to couple the signal from waveguide to microstrip. The insertion loss of this transition fixture which consist of a 50Ω microstrip line and two transition connections was measured from 26.5 to 40 GHz and was used to obtain the performance of the naked amplifier. Figure 3 shows a global view of the test fixture, which consists of two identical branches with their respective transitions and each branch has inside a MMIC amplifier. Figure 4 shows a detail of one MMIC low noise amplifier connected to microstrip lines and to the bias supply networks by gold bonding wires. Microstrip lines are made on Al_2O_3 substrate with thickness 0.254 mm (0.01 inch) and 9.9 dielectric relative constant. Bias supply networks are made up of miniaturized resistors, capacitors and RF blocking networks.

CIRCUIT PERFORMANCE

Two different performances of the amplifier have been obtained for different bias point. One of them for a low noise figure and the other for high gain without spoiling the noise figure too much. The DC power consumption of the amplifier in both performances came near to 30 mW.

Figure 5 shows the simulated and measured noise figure and the associated gain when it is biased for a low noise figure. A value of 1.8 dB was the best measured noise figure at 29.5 GHz with 21.5 dB gain and a return loss of 7.3 dB and 22.5 dB at input and output respectively. In this case the average noise figure was 2.3 dB with an average gain of 20 dB between 28 GHz and 36 GHz. This circuit exhibits a good noise performance in agreement with other works [5]. These simulated results do not include the input and output waveguide-microstrip transitions and all these measurement results have been de-embedded, thanks to the transition fixture measurements. The simulated and measured results are in good agreement as can be seen in this figure.

Figure 6 shows a comparison between the simulated and measured gain and noise figure of the amplifier for higher gain with a small increase in the noise figure. These results do not include the waveguide-microstrip transitions. The maximum gain was 28.9 dB between 30 and 31 GHz with an associated noise figure of 2.5 dB. From 29 GHz to 35 GHz the gain is greater than 25 dB and the average noise is 2.5 dB. The simulated and measured input and output return losses for the same bias point are plotted in Figure 7. There is a slight discrepancy between simulations and measurement at the input and output return losses, but they are basically in good agreement.

CONCLUSIONS

The design and measurements of a fully integrated Ka-band low noise amplifier based on a $0.2 \mu\text{m}$ GaAs PHEMT technology has been described. The circuit has been assembled in a homemade test fixture with waveguide accesses. A minimum noise figure of 1.8 dB was achieved. The average noise figure was 2.3 dB with an average gain of 20 dB between 28 GHz and 36 GHz, with low DC power consumption. From 30 to 31 GHz a gain of 28.9 dB with input return loss better than 15 dB has been measured.

ACKNOWLEDGEMENT

This work has been co-financed by the Spanish “Comisión Interministerial de Ciencia y Tecnología” (CICYT) and the European Commission by the grant reference 1FD97-1769-C04-02. The authors would like to thank to Eva María Cuerno for her assistance in the assembly of this circuit.

REFERENCES

- [1] J. Engberg, “Simultaneous input power match and noise optimization using feedback”, in *Proc. 4th European Microwave Conf.* 1974, pp.385-389.
- [2] K.B. Niclas, “ GaAs MESFET feedback amplifiers: design considerations and characteristics”, *Microwave Journal*, pp. 39-48 & 85, Mar. 1980.
- [3] K.B. Niclas, W. T. Wilser, R. B. Gold & W. R. Hitchens, “The matched feedback amplifier: Ultrawide-band microwave amplification with GaAs MESFETs”, *IEEE Trans. Microwave Theory Tech*, vol. MTT-28, pp.285-294, Apr. 1980.
- [4] Wolfgang J. R. Hofer, “Closed-Form Expressions for the Parameters of Finned and Ridged Waveguides”, *IEEE Trans. Microwave Theory Tech*, vol. MTT-30, pp.2190-2194, Dec. 1982.
- [5] N. Rao, A. Parfitt, A. Dadello, D.Ward, T.Bird, A Low Noise Ka-band Down Converter For Space Applications”, *GAAS 2000 Conference Proceedings*, pp.580-583, Oct. 2000.

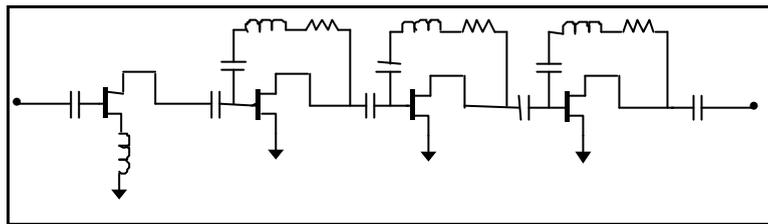


Figure 1. Schematic of the low noise amplifier

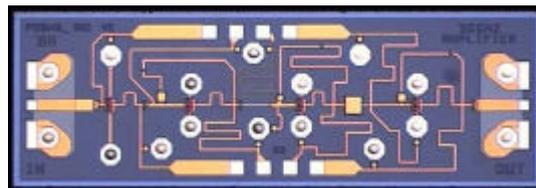


Figure 2. Photograph of the MMIC low noise amplifier

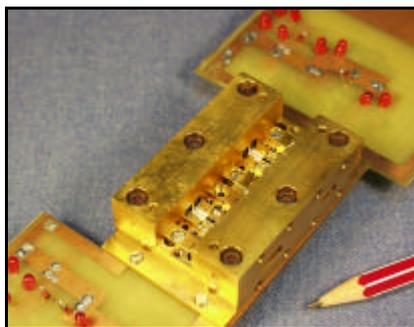


Figure 3. Photograph of the complete test fixture

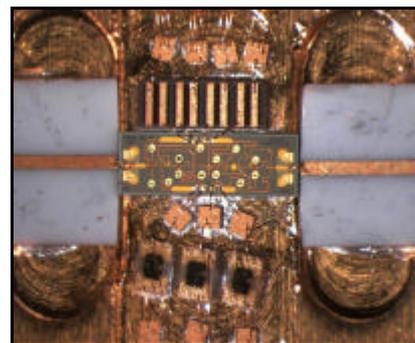


Figure 4. Photograph of the MMIC low noise amplifier assembly

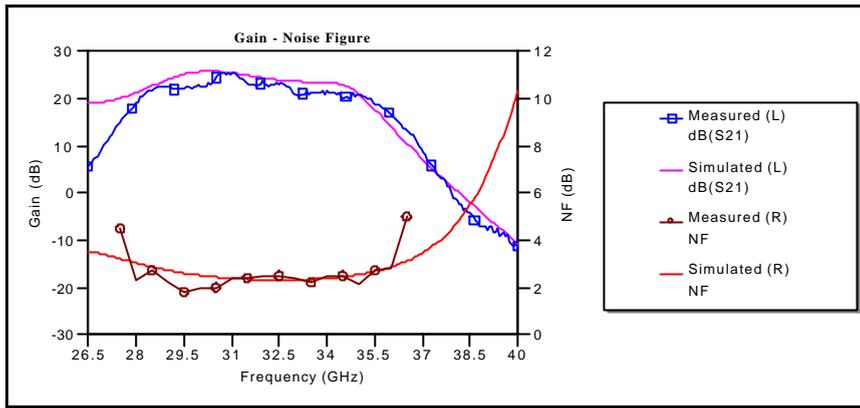


Figure 5. Measurement and simulation of the Gain and Noise Figure Minimum Noise Figure

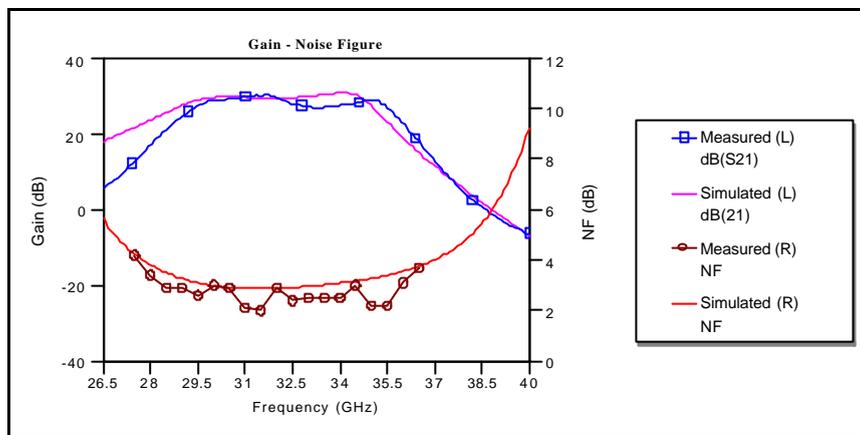


Figure 6. Measurement and simulation of the Gain and Noise Figure Maximum Gain

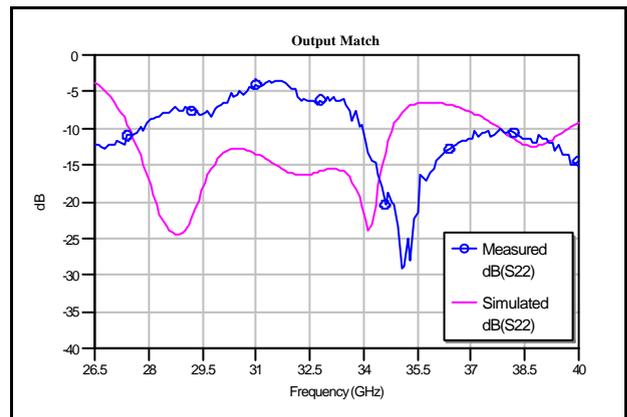
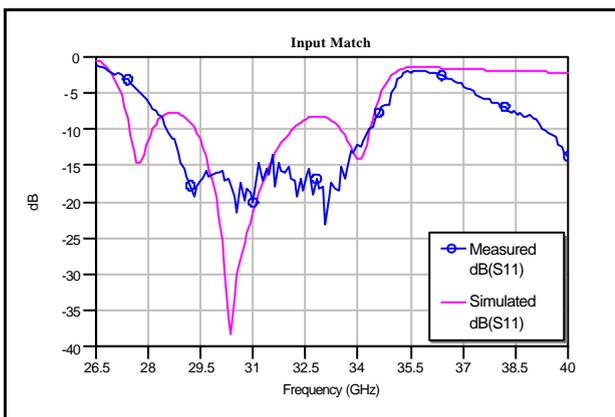


Figure 7. Measured and simulated input and output return loss performance