A FULLY INTEGRATED SILICON-GERMANIUM X-BAND VCO

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Abstract

The design and realisation of a fully integrated Silicon Germanium (SiGe) X-Band Voltage Controlled Oscillator (VCO) is presented. It performs low phase noise and 10% tuning bandwidth at low voltage bias supply. The VCO, comprising integrated inductors and output transformers, is implemented in a SiGe technology which is suitable for high volume production. The features of this VCO, the adopted methodology and the herein proven potential of the technology make this work a good starting point for the design of next generation totally integrated fast PLL's. The paper will describe also the architectures chosen and the design techniques adopted**.**

Introduction

The increasing demand of high-speed high-complex communication systems led to a great interest in the integration of many digital and RF functions on the same chip. Particularly in communication transceivers and 10-Gbit fiber optic systems, the VCO is one of the most critical bulding blocks and is not easily completely integrated. In fact, even when reducing the package and interconnection effects fully integrated LC resonators show a decrease in Quality factors (Q) of varactor diodes and inductors due to higher losses compared to related external components. The best trade-off among electrical performances such as phase noise, gain, current consumption and reliability was the main goal of this work.

Technolgy

The 10GHz VCO is designed with the BiCMOS6G Silicon-Germanium technology from STmicroelectronics also with the aim to investigate the RF capabilities of this process. The BiCMOS6G is a 0.35um SiGe HBT/CMOS suitable for system-on-chip applications. Together with SiGe HBT transistor (whose basic characteristics are listed in TAB.1) the process provides designers NPN BJT's with five metal layers, MIM capacitors and high resistive poly.

Circuit design

The X-Band VCO consists of three basic electrical blocks: oscillator, buffer and transformer (fig.1). The core of the oscillator, which is AC coupled to the following buffer, is a differential pair with a capacitive cross-coupled feedback (fig.2). The differential topology allow a better integration of the designed oscillator in a totally integrated fast PLL. The LC oscillator tank comprises two P+/Nwell varactor diodes and inductors. The inductors were computed by means of the formulas reported in bibliography [1] which also take into account the mutual inductance of close conductors. The calculated inductance was checked with FastHenry (a three dimensional inductance extraction program) which pointed out a 5% difference .

The quality factor of integrated inductors is limited by resistive losses in metal traces and by induced currents both in metal conductors and Silicon substrate [2] [3]. In order to reduce the substrate losses thus improving the Q factor, patterned ground shields were drawn underneath the inductors. The patterned ground shield reduces mutual coupling (in comparison with the solid ground shield) and the impedance to ground providing a good short for the electric field. The metal line width of tank inductors has been optimised to reduce their series resistance.

The value of designed tank inductors is $L = 0.3\,nH$ which provides a central oscillation frequency ω_0 at 10 GHz according to $\omega_0 = 1/\sqrt{LC}$ where C is the equivalent capacitance the tank circuit.

To increase the current source impedance, a further inductor was connected between the emitter feedback resistor and the ground.

In order to achieve a wide tuning range at low voltage bias supply, the VCO must perform a high gain. However the phase noise is also strictly related to the VCO gain (K_{VCO}) and higher is the gain higher becomes the phase noise [4] as pointed out by the following formula:

$$L(f_m, K_{VCO}) = 10\log\left\{\left(\frac{f_0}{2Q\,f_m}\right)^2\left[\left(\frac{FkT}{2P_s}\right)\left(1+\frac{f_c}{f_m}\right)\right]+\frac{1}{2}\left(\frac{K_{VCO}\,V_m}{2\,f_m}\right)\right\}$$

$L(f_m, K_{VCO})$: Phase noise [dBc/Hz]; f_m : frequency offset from the carrier [Hz]; f_0: oscillation frequency [Hz];

F : transistor noise figure; k: Boltzmann's costant [J/K]; T: junction temperature [K]

P_S : RF Output power [W]; f_c: flicker noise corner [Hz]; K_{VCO}: VCO gain corner [Hz/V]

Q_S : tank quality factor; V_m: total low frequency noise [V/Hz]

Thus, the bias point of differential pair of the oscillator, the value of varactor diodes and the layout of inductors were optimised to obtain the best trade-off among phase noise, frequency tuning range and power consumption in all operating points.

The output stage comprises the buffer and a planar transformer designed to decouple the core of the VCO and external load for the reduction of pulling factor.

Particular care has been devoted to the design of the layout drawn with the aim of reducing crosstalk and parasitics. An important work has been done to improve the layout of inductors in order to achieve an optimum Q at operating frequencies.

Measurement and simulation results

Naked chips of the VCO were mounted on Arlon AR1000 substrate (ε_r =9.8) and housed in suitable test jigs (Fig.5). External components such as resistor and capacitors were placed on the board to clean DC bias lines from the noise of bias power suppliers. Single ended measurements were performed connecting the RF signal to the instrumentations and the other to 50-Ohm termination

Figures 6 and 7 show the comparison of simulated and measured results of VCO at nominal operating point in free running mode (18mA of current consumption). The circuit was simulated with SpectreRF and Eldo tools. The main VCO features are 1GHz tuning range and –87dBc/Hz of phase noise @100KHz offset. The good agreement between simulations and measures provides a further validation of the available models and adopted design approach. The slight differences in the results can be traced back to some imprecise parasitic evaluations around the collector nodes of the VCO's core. The VCO is also tested in the bias voltage range 3.0V to 3.6V and at environment temperature range -30°C to 100°C. The measurements carried out a pushing factor of 83MHz/V and a variation of +/-0.95MHz/°C of the central oscillation frequency vs. temperature. The tuning range

remains almost constant (1GHz bandwidth) over bias voltage and temperature variations when the varactor control voltage is between 0.0V and 3.0V.

Bibliography

[1] "Design of planar rectangular microelectronic inductors" H.M. Greenhouse – IEEE Trans. on Parts, Hybrid and Packaging, Vol.10 N.2 June 1974

[2] "On chip spiral inductors with patterned ground shields for Si-based RF IC's" C.P Yue and S.S.Wong- IEEE JSSC vol. 33. No. 5, May 1998]

[3] "Monolithic transformers and their applications in a differential CMOS RF low-noise amplifier" J.J Zhou and D.J. Allstot, IEEE JSSC Vol.33 No. 12, December 1998

[4] "The effect of varactor nonlinearity on phase noise of completely integrated VCO's" J.W.M.Rogers, J.A.Macedo and C.Plett- IEEE JSSC vol. 35. No. 9, September 2000

Parameter	Value
h_{fe}	95
V_{EA}	60 V
BV_{CE0}	3.6 V
C_{BE}	5.0 fF
C_{BC}	3.3 fF
C_{CS}	15.7 fF
F_t	45 GHz
F_{max}	60 GHz

Tab.1-Features of BiCMOS6G SiGe Transistor

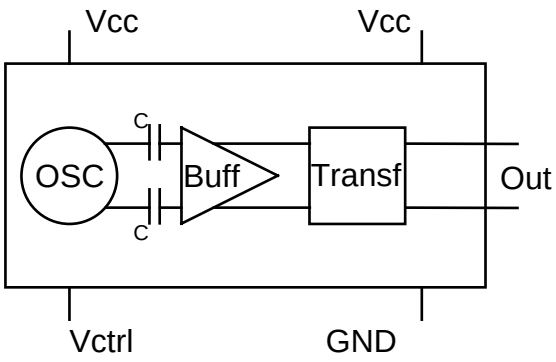

Fig.1-VCO electrical block scheme

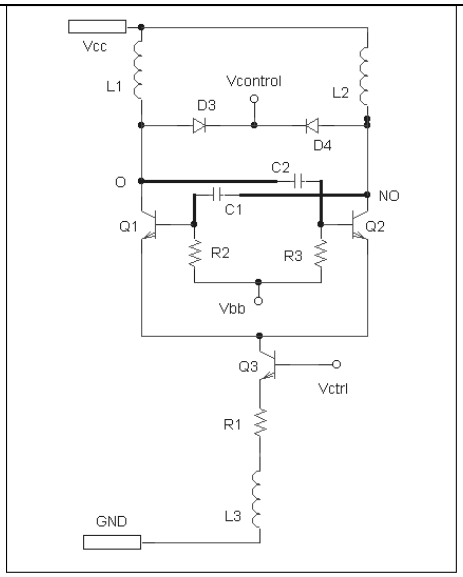

Fig.2- Simplified VCO electrical scheme

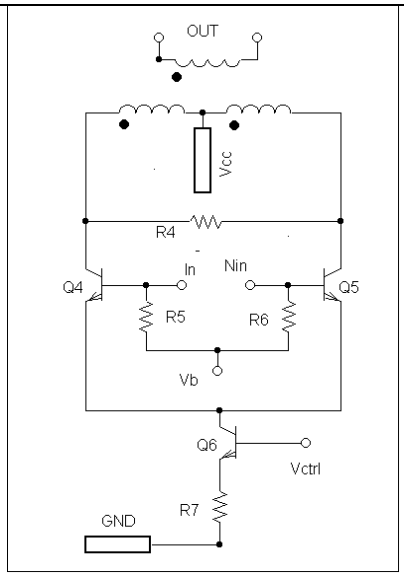

Fig.3- Simplified Buff. and Transformer scheme

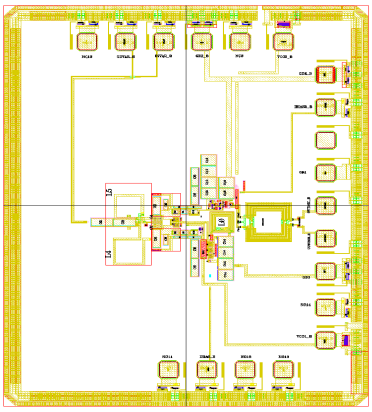

Fig.4- Layout of the SiGe X-BandVCO

Fig.5 -Test jig and bonded naked chip

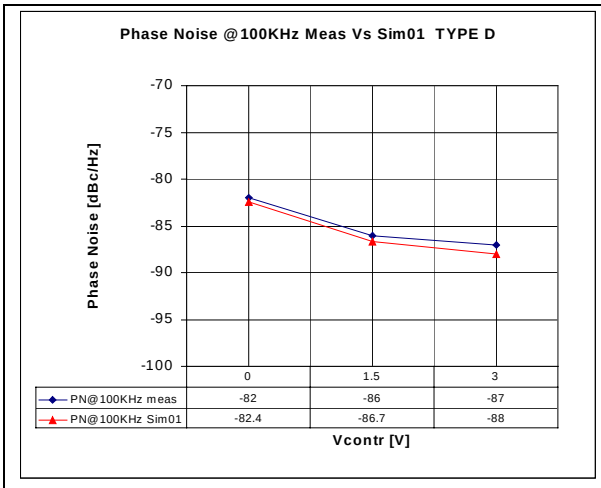

Fig.6- Simulated and measured phase noise

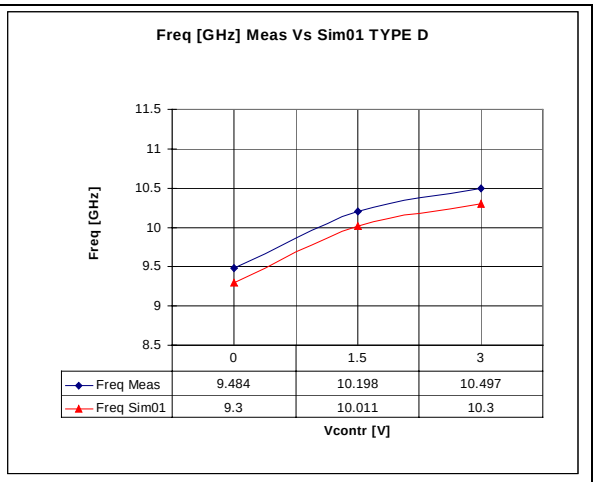

Fig.7- Simulated and measured tuning range